Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6 (Cancelled).

Claim 7 (Previously Presented): A semiconductor device, comprising:

a plurality of capacitor plugs formed within a predetermined interval interleaved between two bit lines and midpoints of capacitor plugs are located at inter-section points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are perpendicular to the X axis virtual lines;

a plurality of lower electrodes of capacitors formed within a predetermined interval to be respectively connected with the capacitor plugs in one to one correspondence,

each lower electrode being octagonally or circularly shaped; and

a plurality of contact pads formed between the lower electrodes and the capacitor plugs, wherein the contact pads are formed over the capacitor plugs and disposed at a lower plane of at least one of the paired lower electrodes.

Claim 8 (Original): The semiconductor device as recited in claim 7, wherein a midpoint of the contact pad is located at an upper plane of the capacitor plug along one of two X virtual axes which is adjacent to each other.

Claim 9 (Original): The semiconductor device as recited in claim 8, wherein a midpoint of the contact pad is deviated from the midpoint of a corresponding capacitor plug but located at a midpoint of the corresponding lower electrode.

Claim 10 (Original): The semiconductor device as recited in claim 8, wherein a midpoint of the contact pad is located at a midpoint of the corresponding lower electrode and the lower electrode corresponding to the contact pad and another lower electrode which is adjacent to the lower electrode corresponding to the contact pad along the Y virtual axis are disposed at positions deviated from the Y virtual axis in an opposite direction.

Claim 11 (Original): The semiconductor device as recited in claim 8, wherein size of the upper plane of the contact pad is greater than that of the upper plane of the capacitor plug.

Claim 12 (Cancelled).

Claim 13 (Previously Presented): A method for fabricating a semiconductor device, comprising:

forming a plurality of capacitor plugs within a predetermined interval interleaved between two bit lines by arranging midpoints of capacitor plugs located at inter-section points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are perpendicular to the X axis virtual lines;

forming a plurality of lower electrodes of capacitors within a predetermined interval to be respectively connected with the capacitor plugs in one to one correspondence, each lower electrode being octagonally or circularly shaped; wherein forming the plurality of lower electrodes comprises:

depositing a sacrifice insulation layer over the capacitor plug formed over a semiconductor substrate;

forming a plurality of open parts exposing the capacitor plugs by performing an selective etching of the sacrifice insulation layer by using a mask pattern;

depositing a material for the lower electrode on an entire profile of the semiconductor substrate comprising the open parts;

forming the lower electrodes separated from each other by performing a planerization process until the sacrifice insulation layer is exposed; and

removing the sacrifice insulation layer by carrying out a wet dip-out process.

Claim 14 (Previously Presented): The method as recited in claim 13, wherein the mask pattern having an open part and neighbored open part disposed along a direction of the Y virtual axis line are formed not to have overlapped area or to have minimum overlapped area, if the open part is moved to the same X virtual axis line as the other open part.

Claim 15 (Previously Presented): The method as recited in claim 14, wherein the mask pattern having the open part and neighbored open part disposed along a direction of the Y virtual axis are not on the same Y virtual axis.

Claim 16 (Previously Presented): The method as recited in claim 14, wherein the mask pattern having the open part and the neighbored open part are not disposed along the same Y virtual axis.

Claim 17 (Original): The method as recited in claim 14, wherein the open part of the mask pattern features an octagonal or a circular shape and a ratio of a major axis to a minor axis of the open part ranges from about 1 to 1 to about 2 to 1.

Claim 18 (Cancelled).

Claim 19 (Previously Presented): A method for fabricating a semiconductor device, comprising:

forming a plurality of capacitor plugs within a predetermined interval interleaved between two bit lines by arranging midpoints of capacitor plugs located at inter-section points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are perpendicular to the X axis virtual lines; and

forming a plurality of lower electrodes of capacitors within a predetermined interval to be respectively connected with the capacitor plugs in one to one correspondence, each lower electrode being octagonally or circularly shaped;

wherein a plurality of contact pads are respectively formed between the lower electrodes and the capacitor plugs after forming the capacitor plugs, wherein the contact pads serve as connecting the lower electrode with the capacitor plug electrically.

Claim 20 (Original): The method as recited in claim 19, wherein the contact pads are formed over the capacitor plugs and midpoints of the contact pads are located at a lower plane of at least one of the paired lower electrodes along the X virtual axis.

Claim 21 (Original): The method as recited in claim 19, wherein the contact pads are disposed on upper planes of the capacitor plugs of which midpoints are located along one of a pair of X virtual axes adjacent to each other.

Claim 22 (Original): The method as recited in claim 20, wherein the midpoints of the contact pads are deviated from the midpoints of corresponding capacitor plugs and respectively located at midpoints of corresponding lower electrodes.

Claim 23 (Original): The method as recited in claim 20, wherein a midpoint of the contact pad is located at a midpoint of the corresponding lower electrode and the lower electrode corresponding to the contact pad and an adjacent lower electrode found along the Y virtual axis are disposed in a way crossing each other.

Claim 24 (Original): The method as recited in claim 20, wherein size of the upper plane of the contact pad is greater than that of the upper plane of the capacitor plug.

Claim 25 (Previously Presented): The semiconductor device as recited in claim 7, wherein a lower electrode and neighbored lower electrode disposed along a direction of Y virtual axis line are formed not to have overlapped area or to have minimum overlapped area, if one of lower electrode is moved to same X virtual axis line of the other lower electrode.

Claim 26 (Previously Presented): The semiconductor device as recited in claim 7, wherein a lower electrode and neighbored lower electrode disposed along a direction of Y virtual axis are not on same Y virtual axis.

Claim 27 (Previously Presented): The semiconductor device as recited in claim 7, wherein the midpoints of a lower electrode and the neighbored lower electrode are not disposed along same Y virtual axis.

Claim 28 (Previously Presented): The semiconductor device as recited in claim 7, wherein a ratio of a major axis to a minor axis of the upper plane of the lower electrodes ranges from about 1 to 1 to about 2 to 1.

Claim 29 (Previously Presented): The semiconductor device as recited in claim 7, wherein an area of an upper plane of a lower electrode is practically identical to that of a lower plane of the lower electrode in view of a three-dimensional structure and the lower electrode features an octagonal or a circular cylinder structure having a lateral plane connecting the upper plane with the lower plane, wherein the lateral plane is practically vertical to the upper plane and lower plane respectively.